VLSI Design and Verification of a CMOS Inverter Using the Tanner EDA: A Case Study

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ABSTRACT

Although the Tanner EDA has been widely used in many universities, there is lack of a shareable publication, document, or tutoring video on VLSI design and verification. Few online tutorials or tutoring video are quite outdated. They either cannot be used for step-by-step guideline, or they only cover part of the entire design flow, which doesn't meet designer's need.

The lack of up to date publication or document has caused a huge barrier for universities to teach a VLSI lab. Due to a severe discrepancy in procedure and parameter setting, instructors have to report technical cases to the Tanner EDA technical support center, and then spend significant time troubleshooting problems with the remote assistance from the Tanner engineers. This has greatly affected the progress of lab teaching and student learning. Therefore, there is an urgent need to create and disseminate a shareable publication or document on VLSI design and verification with the latest version of Tanner EDA.

This paper promotes the needs of a comprehensive study on the newest version of Tanner Tools Pro v16.0 (released in 2013), a state-of-the-art CAD tool for VLSI design. An inverter is used as a proof-of-concept example to go through the major VLSI design flow, including schematic capture, pre-layout simulation, physical layout, extract, design rule check (DRC), and layout vs schematic (LVS). For each step, not only the most challenging and crucial parts are addressed, but also the most different parts from the outdated online tutorial are explained in detail with necessary snapshots. Other universities and designers will find it an invaluable document, which ensures an efficient and fast VLSI design and verification.

Keywords: VLSI Design and Verification, CMOS Inverter, Tanner EDA

1. INTRODUCTION

To keep up with the phenomenal growth in very large scale integration (VLSI) technologies, it is critical for higher education institutions to teach the most competitive computer-aided design (CAD) tools in the market [1][2][3].

Tanner EDA (electronic design automation) is one of the leading EDA industries in the world. It is a powerful and productive analog and mixed-signal ICs design suite that drives innovation for analog IC, mixed signal, and MEMS design [4]. One of the most appealing features is that it provides with Windows based IC design tools, which makes it easy to use. Four tools are integrated in this suite.

- S-Edit: schematic capture tool
- T-Spice: SPICE simulation engine integrated with S-edit
- L-Edit: physical design tool
- LVS: layout vs schematic verification tool

2. MOTIVATION AND CHALLENGES

The education of VLSI design laboratory with Tanner EDA faces challenges. Although the Tanner EDA has been widely used in many universities, there is lack of a sharable publication, document, or tutoring video on VLSI design and verification for students. Few online tutorials or tutoring are quite outdated, since Tanner Tools EDA has major releases every 12-18 months. The tutorials or video that can be found on the internet were written before 2011 [5][6][7][8][9][10]. They either cannot be used for step-by-step guideline due to significant difference from the newest version of Tanner EDA, or they only cover a small part of the entire design flow.

The lack of up to date document has caused a huge barrier for universities to teach a VLSI lab. Due to a severe discrepancy in procedure or parameter setting, instructors have to report technical cases to the Tanner technical support center, and then spend significant time troubleshooting the problem with the remote assistance from the Tanner engineers. This will greatly affect the progress of lab teaching and student learning. Therefore, there is an urgent need to create and disseminate a shareable publication or document on VLSI design and verification with the latest version of Tanner EDA.

This paper promotes the needs of a comprehensive exploration on the newest version of Tanner Tools Pro v16.0 (released in 2013), a state-of-the-art CAD tool for VLSI design. A CMOS inverter is used as an example to go through the major VLSI design flow, including schematic capture, pre-layout simulation, physical layout, extract, design rule check (DRC), and layout vs schematic (LVS). For each step, not only the most challenging and crucial parts are addressed, but also the most different parts from the outdated online tutorial are explained in detail with

necessary snapshots. This effort would provide other universities or designers with an invaluable document to ensure an efficient and fast VLSI design and verification.

The remaining of the paper is organized as follows. Section III describes the schematic design. Section IV illustrates the pre-layout simulation. Section V explains the layout design. Section VI depicts the design rule check (DRC), Section VII describes extract, Section VIII explains the layout vs schematic (LVS), and Section IX gives the conclusions.

3. SCHEMATIC DESIGN

Schematic Design establishes the general scope, conceptual ideas, the scale and relationship of the various program elements. The primary objective of schematic design is to arrive at a clearly defined feasible concept based on the most promising design solutions. It consists of the following fundamental elements.

- Open S-edit platform
- Create a new design
- Add libraries to the design
- Create a new view (under menu Cell)
- Add devices, input & output ports, and supply device (VDD) and a ground device (GND)
- Add a voltage source to provide voltages to VDD and GND

A complete schematic design of an inverter is shown in Fig. 1.

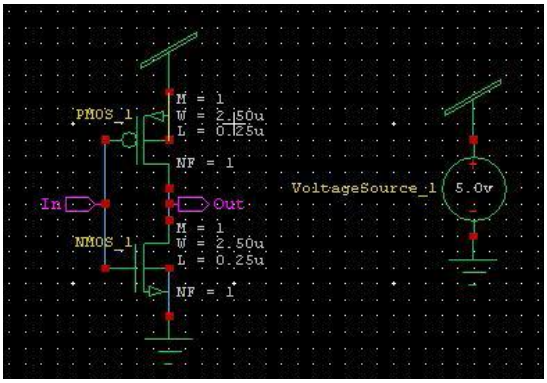

Fig. 1 Circuit schematic of an inverter cell.

4. PRE-LAYOUT SIMULATION

After schematic design, designers have to conduct a pre-layout simulation to check whether their design match with the specification requirement. Assume transient analysis is performed. It includes the following fundamental elements.

- Start S-edit platform
- Open the Inverter design
- Open menu Setup SPICE Simulation, select Transient/Fourier Analysis.
- Select the Generic 250nm library file in the Library Files field. Importantly, TT should be manually added in the end, i.e. Generic_250nm.lib TT, as shown in Fig. 2. It is important to specify the library or model file. Since each MOS transistor symbol fabricated in a different technology will behave differently. Only when a technology process is specified, the MOS transistor symbol can be associated to that process and behavior accordingly.

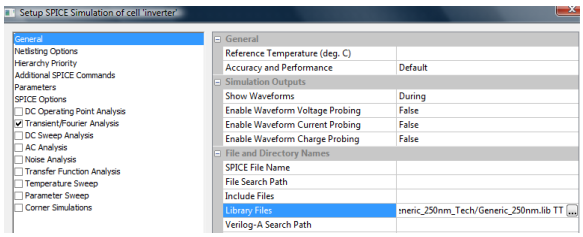

Fig. 2 Make selection of simulation type and set the library files in the Setup SPICE Simulation window.

- Create a pulse voltage source, V2. Under Spice Elements, select voltage source, modify the interface as Pulse. Set the period to 20ns. Drag a Net Label on the higher end of the pulse voltage source, and call it the same name as the input port, i.e. IN.
- To observe the input and output voltages, under Spice Commands, select print voltage, modify the interface to Voltage and create a new instance at the input & output ports. A complete simulation mode circuit schematic is shown in Fig. 3.

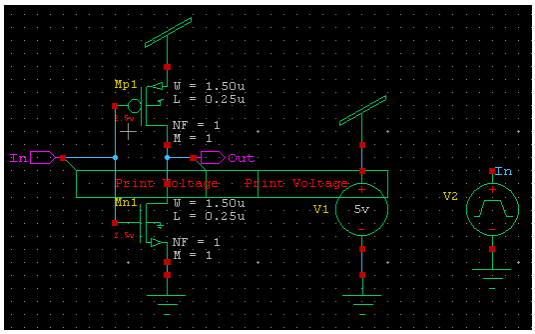

Fig. 3 Simulation mode circuit schematic.

- Run the T-spice simulation. The results of the pre-layout simulation are shown in Fig. 4.

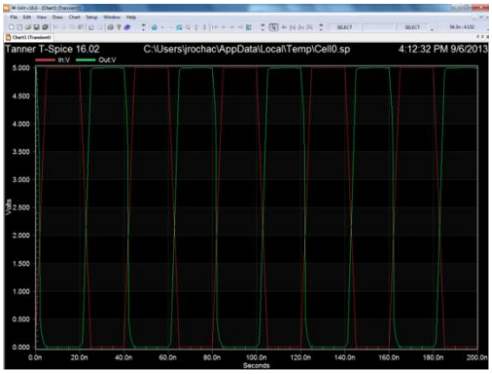

Fig. 4 Pre-layout simulation of an inverter.

5. LAYOUT DESIGN

A layout-design of an IC refers essentially to the three-dimensional character of the elements and interconnections of an IC. There is a continuing need for the creation of new layout designs which reduce the dimensions of existing integrated circuits and simultaneously increase their functions. It consists of the following fundamental elements.

- Open L-edit platform.
- Create a new design. Select TDB as the Technology Reference.
- Add libraries to the design.
- Import Technology.
- Create a new view (under menu Cell).
- Draw the layout.

After adding libraries, all the layers will be added to the layer palette. Designers may use these layers to draw the layout. But designers still have to import technology to your layout design, i.e. Generic_250nm_TechSetup.tdb. Later when you perform DRC check or LVS check, the standard rule set will be checked to see if they have been violated or not. A complete layout of an inverter is shown in Fig. 5.

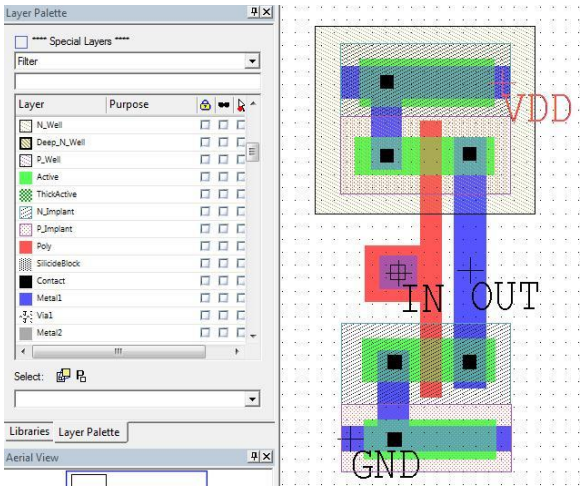

Fig. 5 Layout design of an inverter cell.

6. DESIGN RULE CHECK

Design Rule Check (DRC) is the area of electronic design automation (EDA) that determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called design rules. Design rule checking is a major step during physical verification on the design. Design rules are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of a mask set. Design rules are specific to a particular semiconductor manufacturing process.

Check the DRC Standard Rule Set and run the DRC check. After running DRC, if there is no error that means the design satisfies design rule check, as shown in Fig. 6. Otherwise, check on each rule that is violated, and then go to the location that is circled or marked by bold solid circle or line to fix them.

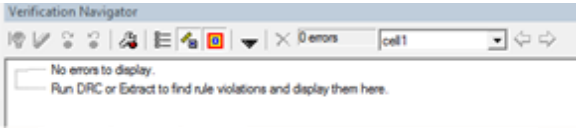

Fig. 6 No error in the DRC rule check.

Usually, the most common errors can be fixed by moving the two layers apart, or adjust the contact size according to the rule.

7. EXTRACT

To verify the functionality and timing of this inverter, the SPICE netlist from the layout needs to be extracted. The extracted view allows designers to run LVS (layout vs schematic). It consists of the following elements.

- Setup extract.
- Unselect HiPer Verify options.
- Extract netlist from the layout.

In the Setup Extract window, use the technology setup from Generic_250 nm.ext file. Designers will see that a SPICE extract output file. i.e. cell1.spc will be generated (in the same folder with their layout) after running the extraction. In addition, if designers do not have HiPer Verify license, they won't be able to use Hierarchical or background settings in Setup Extract. Instead, designers should uncheck all the options under "HiPer Verify" options, as shown in Fig. 7.

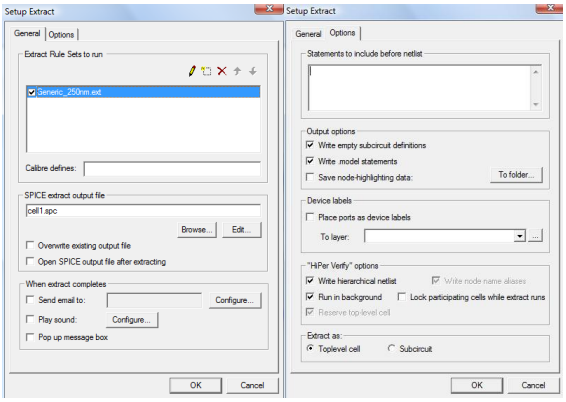

Fig. 7 The Setup Extract window. The left figure shows the definition file under the General tab. The right figure shows the HiPer Verify setting under the Option tab.

8. LAYOUT VS SCHEMATIC (LVS)

The Layout Versus Schematic (LVS) is the class of EDA verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. LVS verification involves:

1. Extraction: The software program takes a database file containing all the layers drawn to represent the circuit during layout. It then runs the database through many area based logic operations. Area based logical operations use polygon areas as inputs and generate output polygon areas from these operations. These operations are used to define the device recognition layers, the terminals of these devices, the wiring conductors and via structures, and the locations of pins (also known as hierarchical connection points).
2. Reduction: In the time of reduction the software combines the extracted components into series and parallel combinations if possible and generates a netlist representation of the layout database. A similar reduction is performed on the "source" schematic netlist.
3. Comparison: The extracted layout netlist is then compared to the netlist exported from the circuit schematic. If the two netlists match, then the circuit passes the LVS check and a message will come "Circuits are equal". The procedure includes the following elements.

- Open LVS platform
- Create a new LVS setup file
- Export SPICE netlist of the schematic from S-Edit. Use this SPICE file for schematic netlist.
- Use the SPICE netlist from previous extraction for layout netlist. The SPICE netlist extracted from the layout and the exported SPICE netlist from the schematic are shown in Fig. 8.

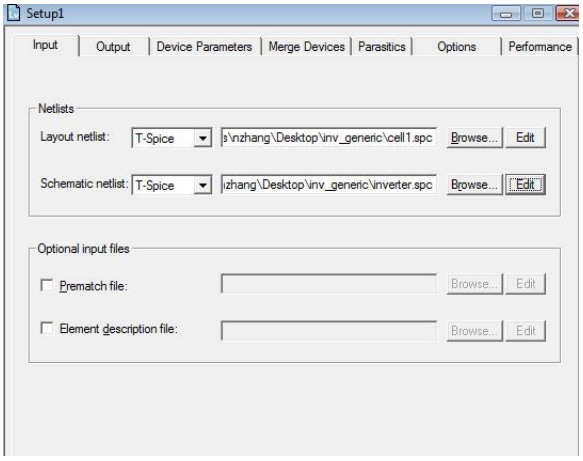

Fig. 8 Layout Versus Schematic (LVS) setup. The SPICE netlist extracted from the layout and the exported SPICE netlist from the schematic are the two inputs.

- Run the verification.

If everything matches, designers will see a report window that says "Circuits are equal" in red, as shown in Fig. 9. If they don't match, it will show which line in the SPICE file is wrong.

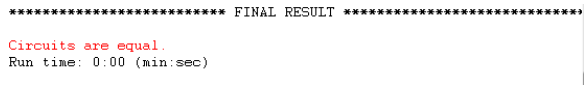

Fig. 9 Layout Versus Schematic (LVS) result. The two circuits are proved to be equal.

9. CONCLUSIONS

This paper thoroughly investigated the design flow of a proof-of-concept CMOS inverter using the latest version of Tanner EDA, i.e. Tanner Tools v16.0, a state-of-the-art CAD tool for VLSI design. It filled in the gap between the outdated tutorials and the up to date document about the latest Tanner EDA. The major VLSI design flow components, including schematic design, pre-layout simulation, physical layout, extract, design rule check (DRC), and layout vs schematic (LVS) were completely explored. For each step, not only the most challenging and crucial issues were addressed, but also the most different parts from the outdated online tutorials or videos were explained in detail with necessary snapshots. This effort would provide other universities and designers with an invaluable document to ensure an efficient and fast VLSI design and verification. In the future, this shareable document will be updated and disseminated on a regular basis to keep up with advances in Tanner EDA technology.

In addition, the proposed study will leverage the key success factors for fresh engineering graduates by equipping them with a rich set of skills to overcome the challenges caused by emerging techniques and rapid changing products.

10. REFERENCES

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