Low Voltage High-Q CMOS Active Inductor For RF Applications

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ABSTRACT

In this paper, an improved design of a high-Q factor CMOS active inductor operating in the mid MHz frequency range is introduced. Analysis of equations has been used to gain insight into behavior of the active inductor. Moreover, based on these equations and their analysis, ways of improving quality factor are discussed. Performance improvement based on this new design coupled with use of feedback series resistor and external capacitor are shown and analyzed. Simulation results and performance improvement are compared and contrasted in the CMOS AMI 0.5u Process based on existing literature. CMOS active inductors have found increasing applications in high-speed analog signal processing and data communications circuits due to the inability of on-chip spiral inductors to scale with technology. Its vast range of applications includes impedance matching circuits, filter circuits, oscillators, and lumped element power dividers.

Keywords: CMOS, RF communication, inductor, feedback, quality factor, gyrator-C

INTRODUCTION

Traditionally the inductor has been used as a discrete component in the communication systems. The integration of the RF and microwave system on a single chip has been the dominant force to have an active inductor that can be easily integrated on a CMOS chip This active inductor can be used in many system components such as filters, amplifiers, mixers, oscillators, etc The initial push for inductor to become integrated part of the chip has produced CMOS spiral inductor. One inherent drawback of a spiral inductor is the low resistivity of silicon substrate that results in the low Q-factor. The planar spiral and multilayer inductor has small inductance value per area and low quality factor due to wiring and substrate losses [9] Active inductor is another option of replacing inductor on a chip. In spite of the inherent drawbacks of active inductors such as noise, linearity, and power consumptions, it has been studied and applied to many RF circuit designs because of its advantages of low insertion loss, small size, and tunability of inductance [10].

Although passive inductor has better performance in terms of noise, power consumption and dynamic range but CMOS active inductor has many attractive features for use in RF and microwave application that are advantages at many applications. CMOS active inductors can provide high quality factor, wide tunability, large inductance, easier integration with less die area.

In this work, an optimized active inductor is presented. The purpose of these adopted optimization techniques has been to reduce the parallel resistance as well as the parasitic resistance that both significantly affect the Q – factor of the active inductor.. Based on information gained through analyzing the model and its equations, feedback elements and cascode structure are used in order to increase the Q – factor of the active inductor.

GYRATOR-C INDUCTOR DESIGN

The gyrator, also called the positive impedance inverter is an active two port network capable of simulating inductance. The Gyrator – C structure is a well known circuit topology to synthesis active inductors. It consists of two back to back connected transconductors, one that has a negative transconductance, another that has a positive transconductance and an external shunt capacitor C.

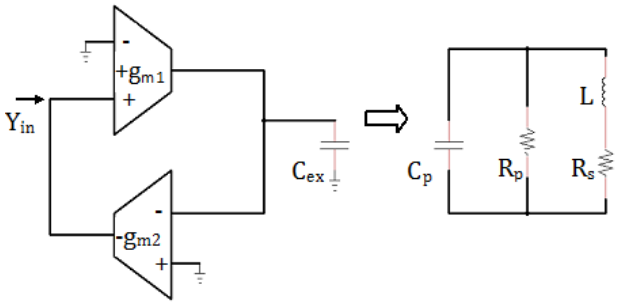

Fig.1. Gyrator – C topology and its RLC equivalent

Fig.1. Also depicts its equivalent RLC model. In the analysis of these structures when we include input and output conductances of the respective transconductors, the gyrator – C behaves as a lossy inductor with parasitic parallel resistance R_p, parallel capacitance C_p and series resistance R_s [2] where the effective resonant frequency of the active inductor is:-

$$\omega_0 = \frac{1}{LC_p}$$

ACTIVE INDUCTOR DESIGN

The active inductor design based on the gyrator-C approach with both the transconductors realized using the common source configuration is shown in Fig. 2 [1]. The current source has been replaced by a transistor with V_{bias} controlling the current magnitude.

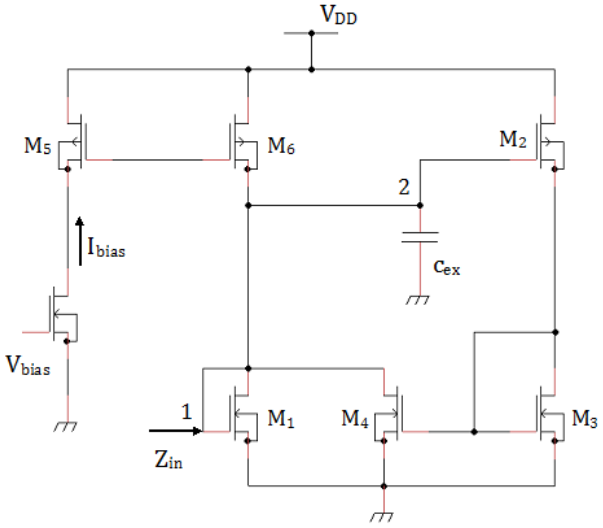

Fig.2. Single-ended active inductor with both transconductors in common source configuration [1]

Analysis of the above circuit to obtain the component values has been done using a lossy single-ended gyrator – C topology shown in fig. 3, with the equivalent conductance and capacitance shown at both nodes. The admittance, rather than the impedance of the circuit below has been obtained for the sake of simplicity.

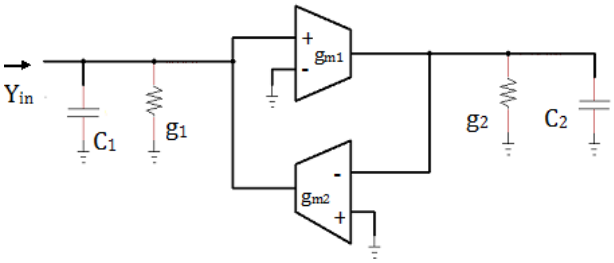

Fig.3. Lossy gyrator architecture

The simplified expression for input admittance is as follows

$$Y_{in} = g_1 + sC_1 + \frac{g_{m1}g_{m2}}{sC_2 + g_2} \qquad (1)$$

The third term in Eq. (1) behaves as an inductor with resistive loss where [3],

$$L = \frac{C_2}{g_{m1}g_{m2}}, \qquad R_S = \frac{g_2}{g_{m1}g_{m2}}$$

And $C_2 = C_{ex} + C_{i2}$ from [1]

$C_1 = C_{i1} + C_{o2}$ from [1]

OPTIMIZATION TECHNIQUES

The parallel resistance R_P observed in the RLC equivalent circuit of an active inductor in Fig. 1 lowers the Q – factor of the active inductor. The following topology in fig. 4 boosts the Q – factor of the active inductor by reducing the parallel resistance R_P.

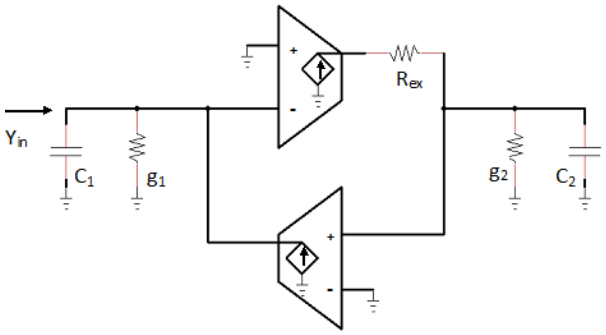

Fig.4. Lossy gyrator architecture with feedback resistance

Using the Miller Theorem, the modified input admittance of the lossy gyrator architecture due to the resistance in the feedback path can be shown as:-

$$Y_{in} = g_1 + sC_1 + \frac{g_{m1}g_{m2}}{sC_2(1 + g_{m1}R_{ex}) + g_2} \qquad (2)$$

The new expressions of the component values obtained from the above eq. (2) are as follows:-

$$L = \frac{C_2(1 + g_{m1}R_{ex})}{g_{m1}g_{m2}}, \qquad R_S = \frac{g_2}{g_{m1}g_{m2}}$$

The above equations indicate an increase in the inductance value by the factor of $(1 + g_{m1}R_{ex})$ as long as $(1 + g_{m1}R_{ex})$ > 1.

The other component that significantly affects the quality factor is the series (parasitic) resistance R_s, which has to be minimized. Techniques that can be used to reduce R_s include increasing the transconductance values of either or both transconductors, increasing the output impedance of the transconductors or introduction of shunt negative resistors to nullify the parasitic resistances [2]. An increase in I_{bias} or transistor widths can be used to boost the transconductance values at the cost of increased static power consumption or decreased self-resonant frequency respectively. For the active inductor in fig. 2 a shunt negative resistor may need a higher transistor count as compared to a simple cascode. The optimized active inductor topology with the series feedback resistance and cascode circuit are shown in fig. 5. The minimum voltage required for proper circuit operation in fig. 5 is $2V_{gs} + V_t$ as compared to $V_{gs} + V_t$ required for [1]. Hence we don't observe a drastic increase in the minimum voltage requirement, which is why it can still be used in low voltage applications.

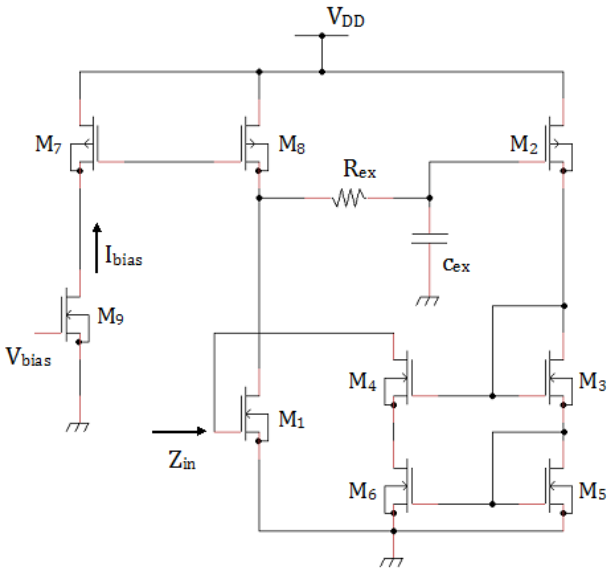

Fig.5. Optimized Transistor level implementation of active inductor topology

SIMULATIONS

An S-parameter analysis of the circuit in [1] and our improved circuit topology was run in the AMI 0.5u CMOS process to find the variation of its input impedance and phase with respect to frequency.

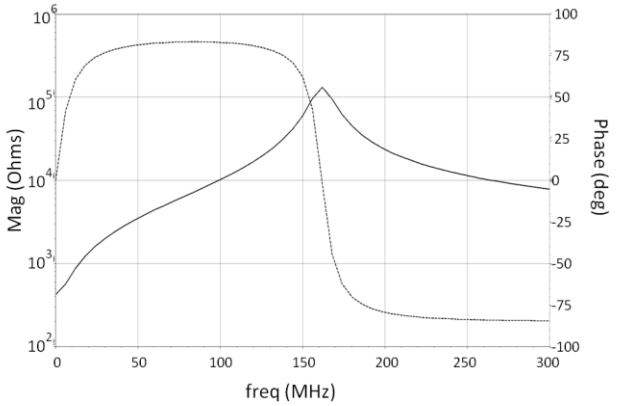

Fig.6a. Simulation of [1] in CMOS AMI 0.5u with Q = 13.2

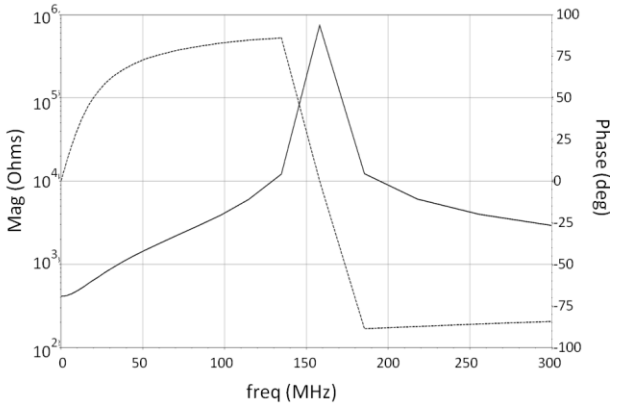

Fig.6b. Simulation of optimized active inductor circuit in CMOS AMI 0.5u with Q = 38

A comparison of simulations in fig 6a and 6b indicate a three-fold increase in the Q – factor of the improved circuit.

Inductance tuning can be obtained by either using a varactor to vary the external shunt capacitor or by varying I_{bias} to effectively vary the transconductance of the transconductors. Fig.7 shows the variation in Q as I_{bias} is varied.

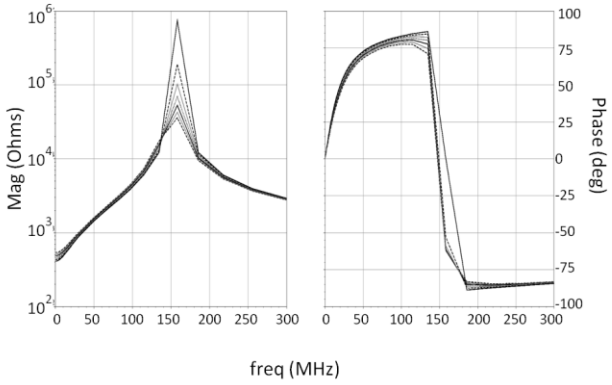

Fig.7. Inductance tuning of the optimized circuit, where I_{bias} is varied from 136u to 141u

NOISE ANALYSIS

Active inductors exhibit a high level of noise as compared to spiral inductors [2]. We can obtain the equivalent output noise from the analysis of the circuits shown below in fig. 8 [2][8]:-

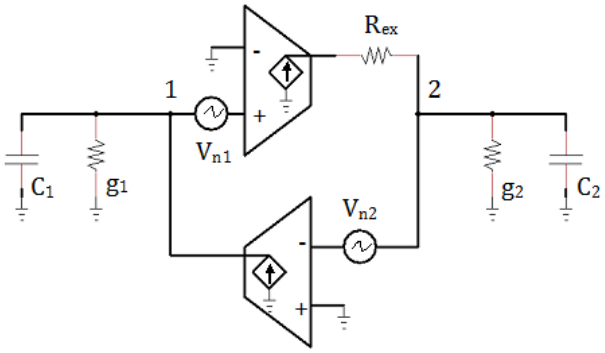

Fig.8a. Gyrator – C topology with noise sources

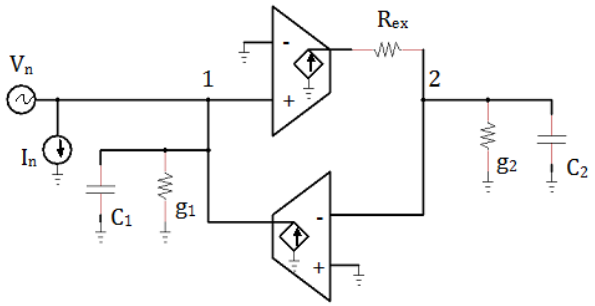

Fig.8b. Gyrator – C topology with equivalent input noise sources

To achieve equivalence between Fig. 3a and 3b we impose the following conditions:-

$$V_n = V_{n1}$$

$$I_n = (g_1 + sC_1)V_{n1} + g_{m2}V_{n2}$$

Because,

$$Y_{in}(s) = \frac{g_{m1}g_{m2}}{C_2(1+g_{m1}R_{ex})}$$

We observe,

$$V_n = V_{n1} + \frac{I_n}{Y_{in}}$$

The above equation shows that V_n is directly proportional to the magnitude of R_{ex}.

Assuming V_{n1} and V_{n2} are uncorrelated, we observe

$$\overline{V_n}^2 = \overline{V_{n1}}^2$$

$$\overline{I_n}^2 = |g_1 + j\omega C_1|^2 \overline{V_{n1}}^2 + {g_{m2}}^2 \overline{V_{n2}}^2 \qquad (3)$$

From Eq.(3), we see that the equivalent output noise is directly proportional to R_{ex}.

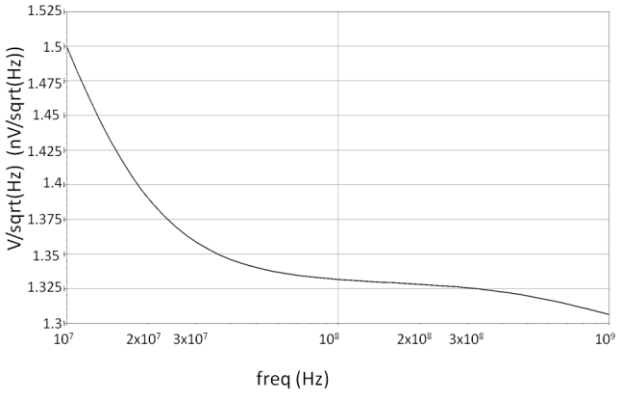

Fig.9a. Noise performance of [1]. Noise = $1.32nV/\sqrt{Hz}$ at a self-resonant frequency of 160MHz

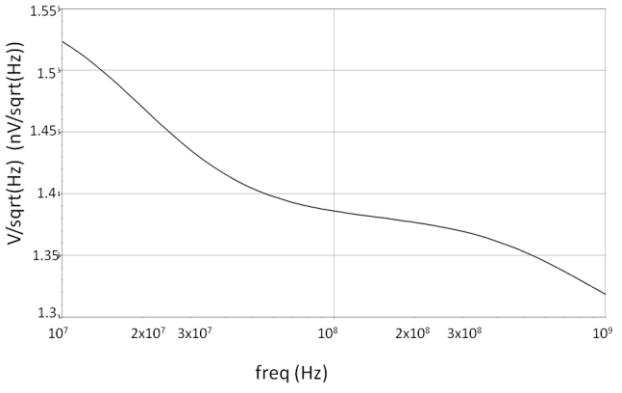

Fig.9a. Noise performance of optimized active inductor. Noise = $1.38nV/\sqrt{Hz}$ at a self-resonant frequency of 160MHz for an external resistor of $200\,\Omega$

CONCLUSION

This paper presents the comparison of two active inductor structures, both simulated in the AMI CMOS 0.5u process. The optimized structure indicates a three-fold increase in the Q – factor at the expense of a negligible increase in noise. The power dissipation of the active inductor circuit in this paper is as low 2.18mW, not much higher than the dissipation in [1] which is 1.06 mW.

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